

INV100EQ030A

100V Bi-directional Enhancement-mode Power Transistor

INV100EQ030A

1. General description

Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in En-FCQFN with 4.0 mm x 6.0 mm package size.

2. Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance

3. Applications

- BMS battery protection
- High side load switch in bi-directional converter
- Switch circuits in multiple power supplier system

4. Key performance parameters

Table 1 Key performance parameters at $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DD, \max}$	100	V
$R_{DD(\text{on}), \max} @ V_G = 5\text{ V}$	3.2	m Ω
$Q_{G, \text{typ}} @ V_{DD} = 50\text{ V}$	90	nC
$I_{D, DC}$	100	A

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Drain1	Power Drain1
8,10,12-20,22,24	Drain2	Power Drain2

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INV100EQ030A	En-FCQFN 4X6	J29

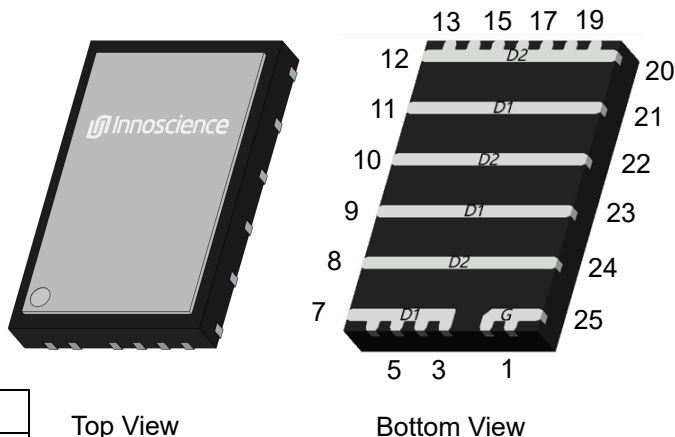
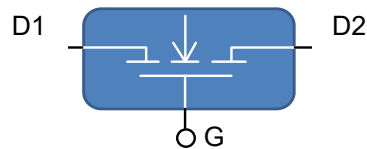


Table of contents

1. General description	1
2. Features	1
3. Applications.....	1
4. Key performance parameters.....	1
5. Pin information.....	1
6. Maximum ratings.....	3
7. Thermal characteristics.....	4
8. Electric characteristics.....	5
9. Electric characteristics diagrams.....	7
10.Package outlines.....	12
11.Reel information.....	13
12.Land pattern	14
13.Revision history	15

6. Maximum ratings

at $T_J = 25\text{ °C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	100	V
$V_{DD(tr)}$	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage (up to 300,000 5ms pulse at 150 °C)	120	V
V_{DG}	Drain1-to-Gate Voltage or Drain2-to-Gate Voltage	100	V
V_{GD}	Gate-to-Drain1 Voltage or Gate-to-Drain2 Voltage	6	V
I_D	Continuous Drain Current	100	A
I_{DM}	Pulsed Drain Current (25°C, $T_{Pulse} = 100\text{ }\mu\text{s}$)	320	A
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	°C

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.24	°C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.31	°C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ¹	56.63	°C/W	-
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{D1D2}	Drain1-to-Drain2 Breakdown Voltage	100	-	-	V	$V_{D2} = V_G = 0\text{ V}$, $I_{D1D2} = 500\text{ }\mu\text{A}$
BV_{D2D1}	Drain2-to-Drain1 Breakdown Voltage	100	-	-	V	$V_{D1} = V_G = 0\text{ V}$, $I_{D2D1} = 500\text{ }\mu\text{A}$
I_{D1D2}	Drain1-to-Drain2 Leakage	-	1	4	μA	$V_{D2} = V_G = 0\text{ V}$, $V_{D1} = 80\text{ V}$
I_{D2D1}	Drain2-to-Drain1 Leakage	-	1	4	μA	$V_{D1} = V_G = 0\text{ V}$, $V_{D2} = 80\text{ V}$
I_{GD}	Gate-to-Drain Forward Leakage	-	1	4	μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = 5\text{ V}$
	Gate-to-Drain Forward Leakage	-	2	8	μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = 6\text{ V}$
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{D1} = 0\text{ V}$, $V_{D2} = V_G$, $I_{D2D1} = 13\text{ mA}$
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{D2} = 0\text{ V}$, $V_{D1} = V_G$, $I_{D1D2} = 13\text{ mA}$
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance	-	2.5	3.2	$\text{m}\Omega$	$V_{D2} = 0\text{ V}$, $V_{GD} = 5\text{ V}$, $I_{D1D2} = 25\text{ A}$
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance	-	2.5	3.2	$\text{m}\Omega$	$V_{D1} = 0\text{ V}$, $V_{GD} = 5\text{ V}$, $I_{D2D1} = 25\text{ A}$

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance	-	3300	-	pF	V _G = 0 V, V _D = 50 V
C _{OSS}	Output Capacitance	-	830	-		
C _{RSS}	Reverse Transfer Capacitance	-	400	-		
R _G	Gate Resistance	-	5	-	Ω	f = 5 MHz, open drain
Q _G	Total Gate Charge	-	90	-	nC	V _D = 50 V, V _G = 5 V, I _D = 25 A
Q _{GD1}	Gate-to-Drain1 Charge (V _{D2D1} =50V)	-	7	-		V _{D1} = 0, V _{D2} = 50 V, I _{D2D1} = 25 A
Q _{GD1}	Gate-to-Drain1 Charge (V _{D1D2} =50V)	-	65	-		V _{D2} = 0, V _{D1} = 50 V, I _{D1D2} = 25 A
Q _{GD2}	Gate-to-Drain2 Charge (V _{D1D2} =50V)	-	7	-		V _{D2} = 0, V _{D1} = 50 V, I _{D1D2} = 25 A
Q _{GD2}	Gate-to-Drain2 Charge (V _{D2D1} =50V)	-	65	-		V _{D1} = 0, V _{D2} = 50 V, I _{D2D1} = 25 A
Q _{OSS}	Output Charge	-	90	-		V _G = 0 V, V _D = 50 V

9. Electric characteristics diagrams

at $T_J = 25^\circ\text{C}$ unless otherwise specified.

Note: In Charts, VD1D2 can be VD2D1 with same characteristic chart due to Bi-directional feature.

Fig. 1 Typical Output Characteristics ($T_J=25^\circ\text{C}$)

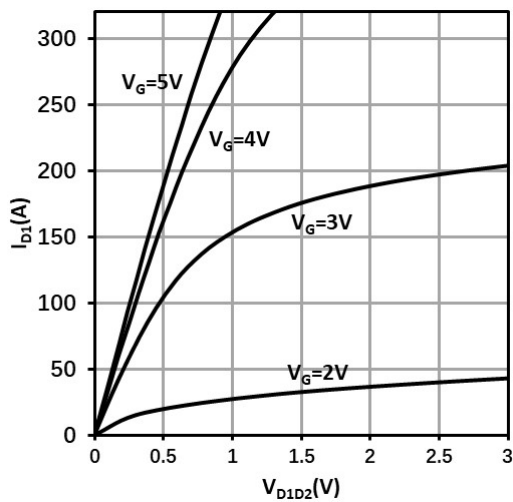


Fig. 2 Typical Output Characteristics ($T_J=125^\circ\text{C}$)

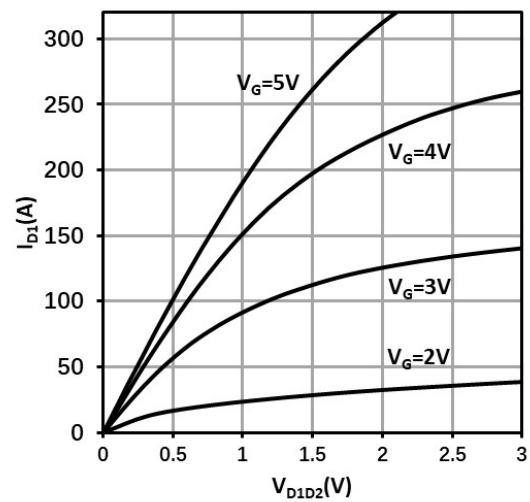


Fig.3 Typical Drain On-state Resistance ($T_J=25^\circ\text{C}$)

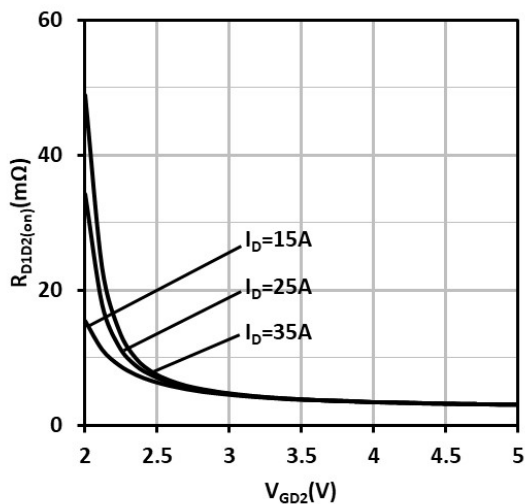


Fig. 4 Typical Drain On-state Resistance ($T_J=125^\circ\text{C}$)

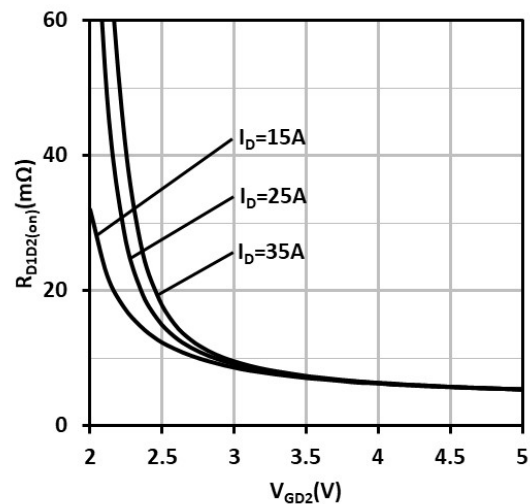


Fig. 5 Normalized On-State Resistance vs. Temp.

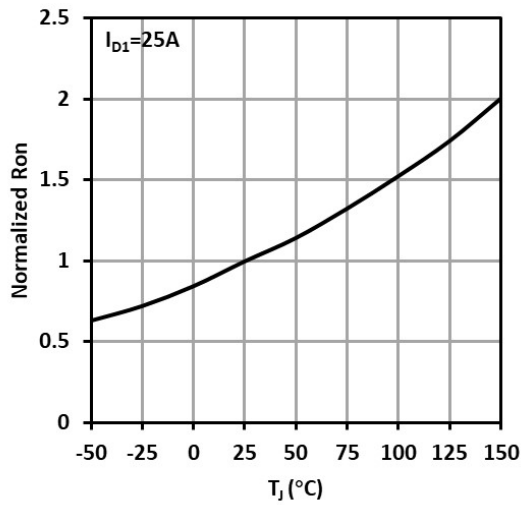


Fig. 6 Typical Transfer Characteristics

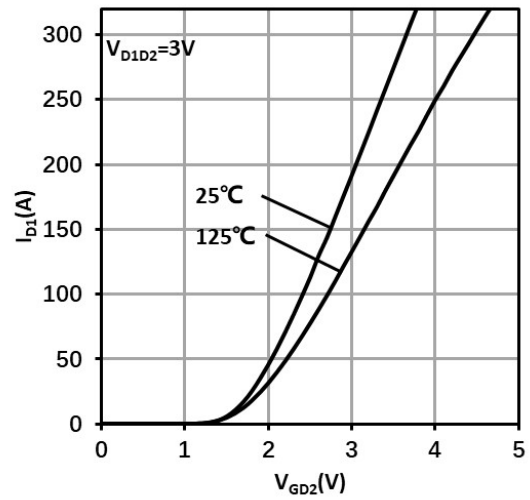


Fig. 7 Typ. Reverse Drain1-Drain2 Characteristics ($V_{GD2} \leq 0, T_J = 25^\circ\text{C}$)

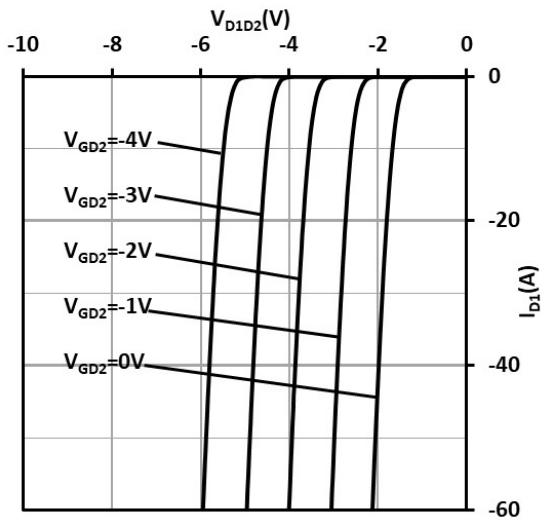


Fig. 8 Typ. Reverse Drain1-Drain2 Characteristics ($V_{GD2} \geq 0, T_J = 25^\circ\text{C}$)

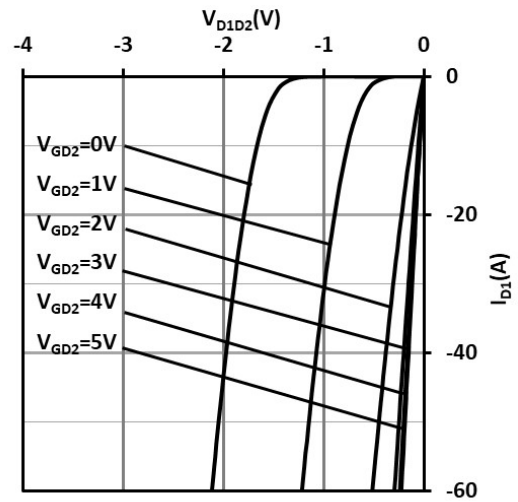


Fig. 9 Typ. Reverse Drain1-Drain2 Characteristics ($V_{GD2} \leq 0, T_J = 125\text{ }^\circ\text{C}$)

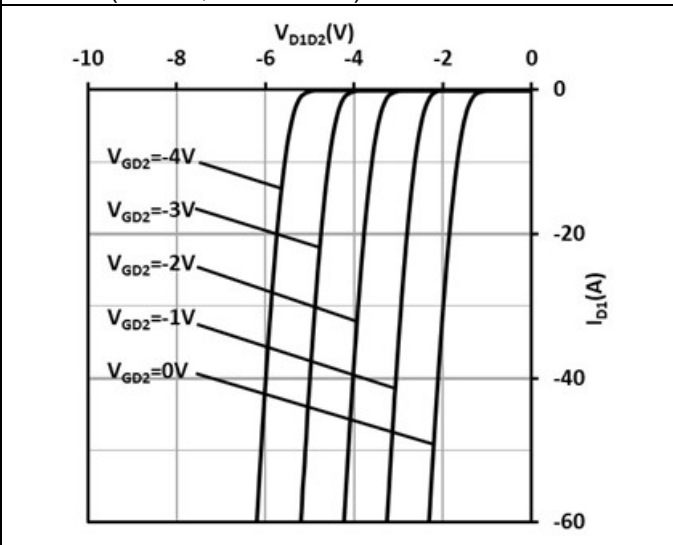


Fig. 10 Typ. Reverse Drain1-Drain2 Characteristics ($V_{GD2} \geq 0, T_J = 125\text{ }^\circ\text{C}$)

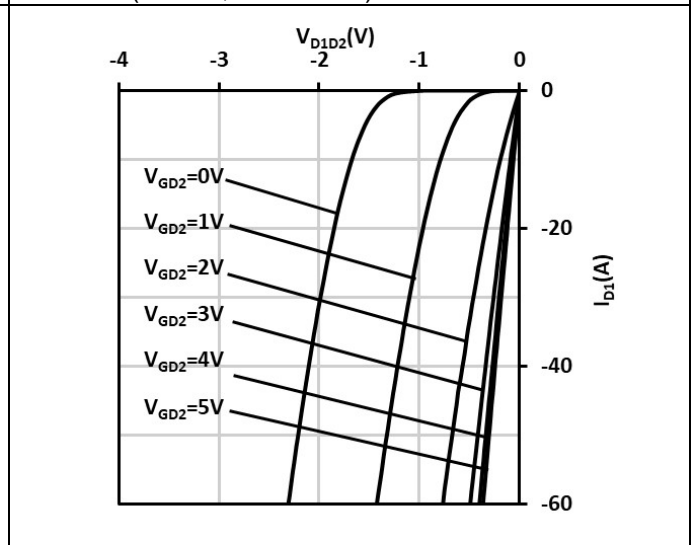


Fig. 11 Typ. Capacitances Characteristics

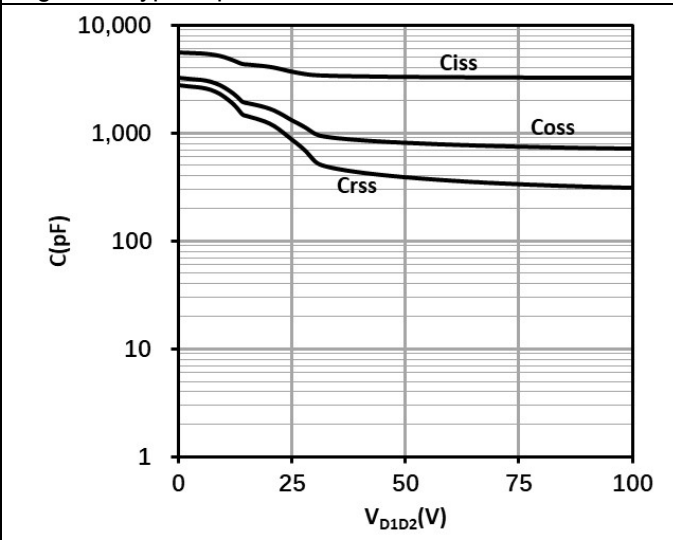


Fig. 12 Typ. Gate Charge

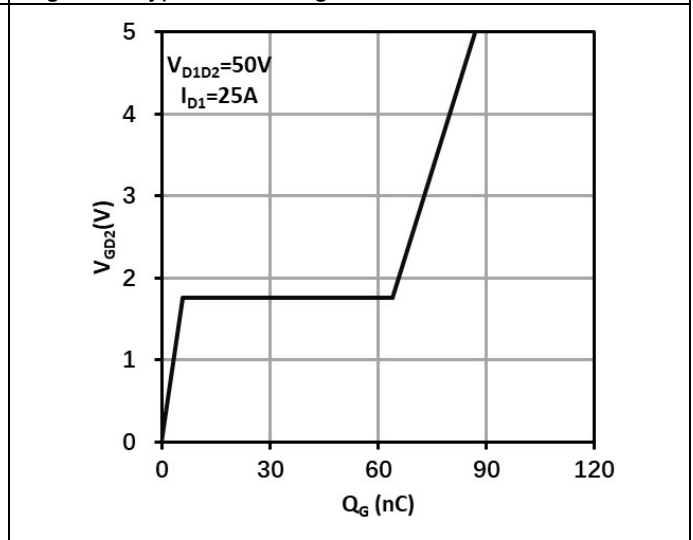


Fig. 13 Normalized Threshold Voltage vs. Temp.

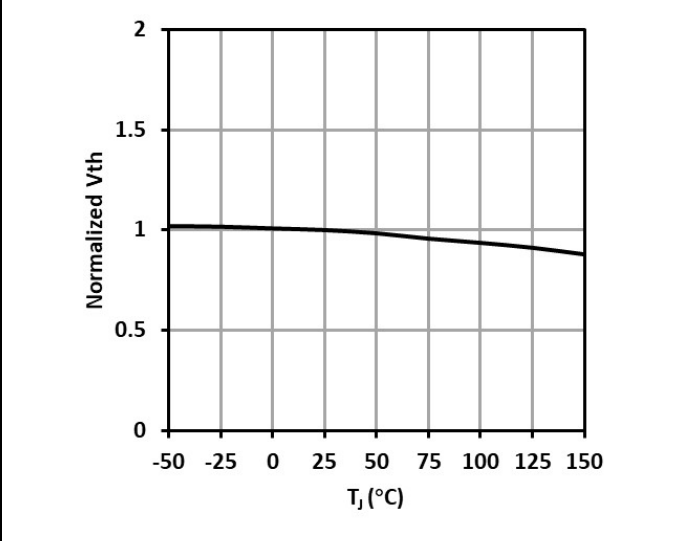


Fig. 14 Output Charge

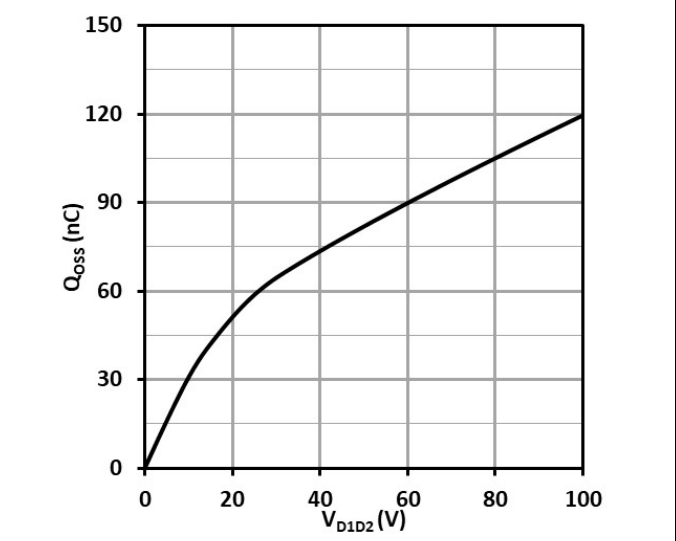


Fig. 15 Output Capacitance Stored Energy

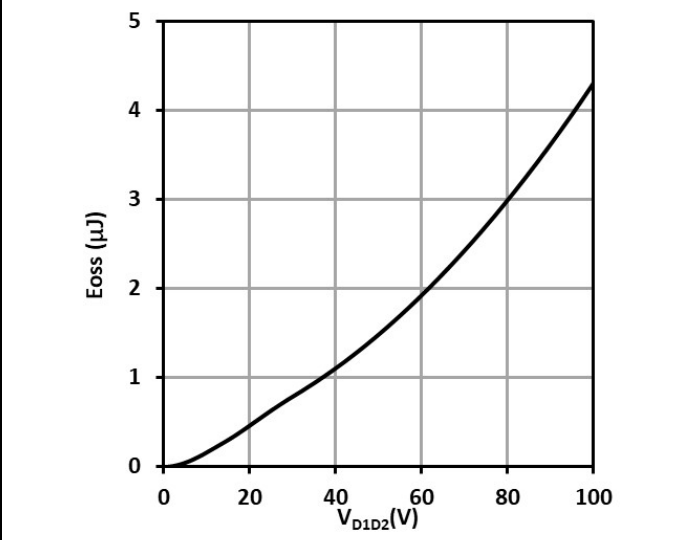


Fig. 16 Power Dissipation

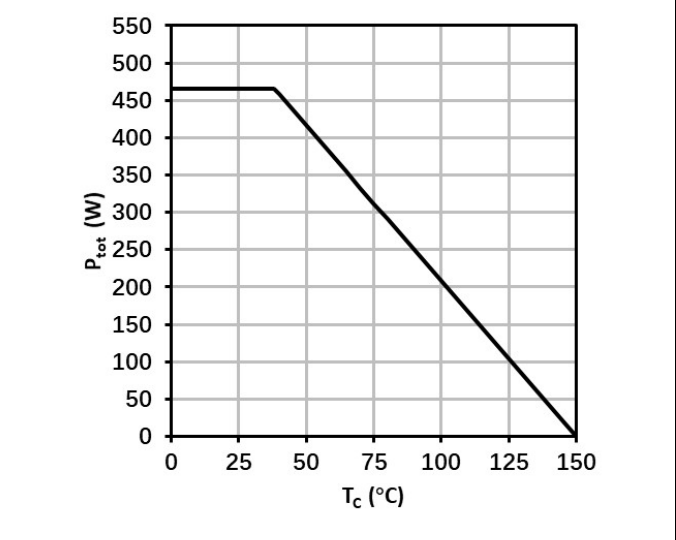


Fig. 17 Safe Operating Area

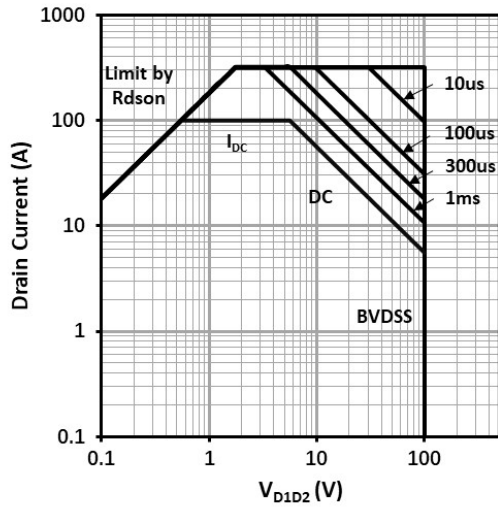
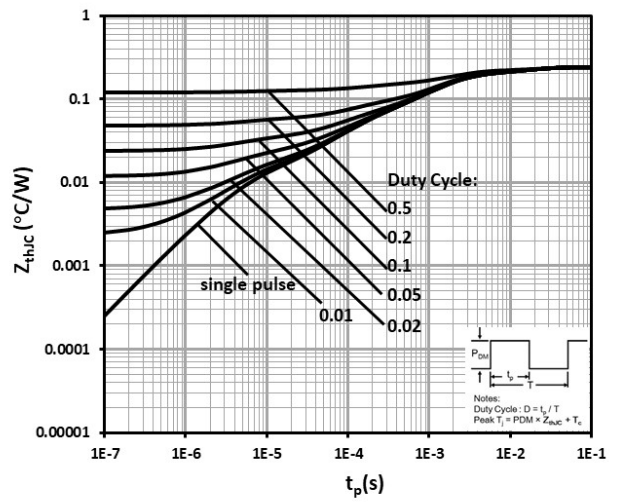
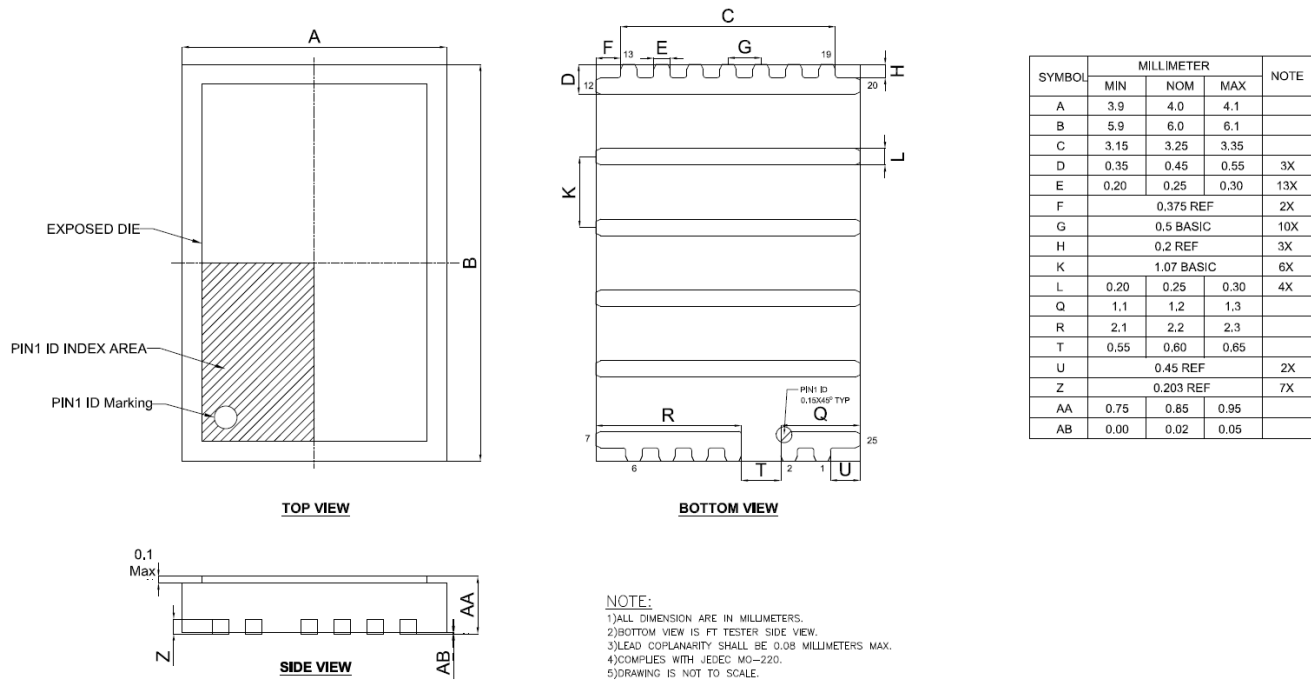


Fig. 18 Max. Transient Thermal Impedance

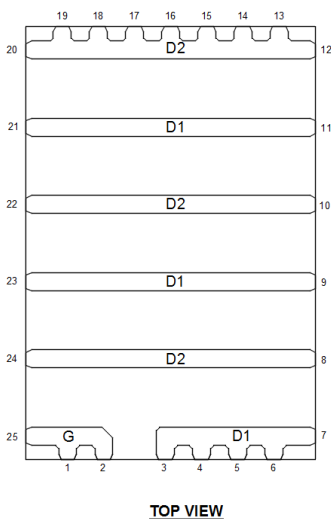


10. Package outlines

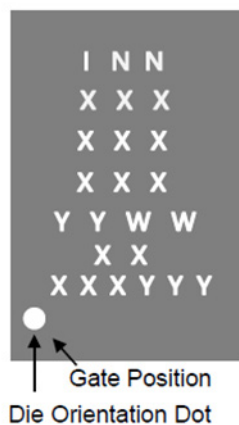
Package Reference



PIN configuration



Marking Reference



Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Lot Code	XXX
Row4		XXX
Row5	Date code	YYWW
Row6	Wafer ID	XX
Row7	Location ID	XXXYYY

11. Reel information

NOTES:

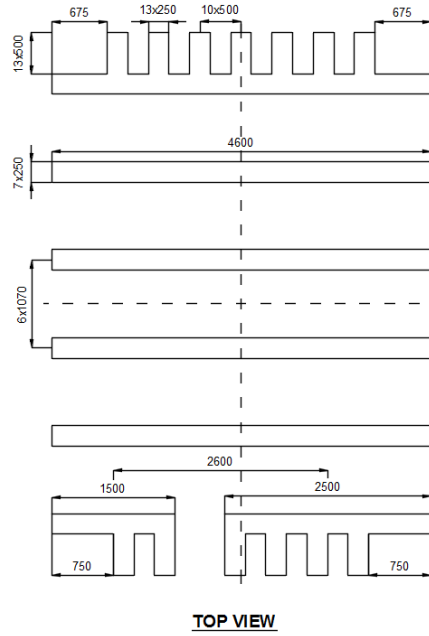
1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.

NOTES:

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

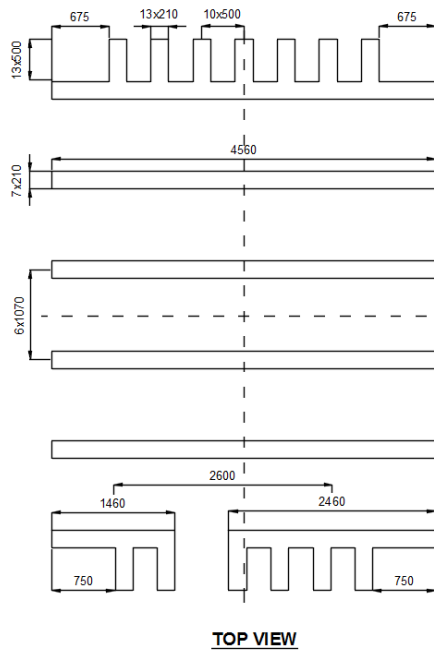
12. Land pattern

Recommended Land Pattern



Unit: μm

Recommended Stencil drawing



Unit: μm

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-02-29	1.0 Version Release

Important Notice

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